FIFO Systems with Interleaved Regulators

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Contents

Abstract: We define the minimal interleaved regulator, which generalizes the Urgency Based Shaper that was recently proposed by Specht and Samii as a simpler alternative to per-flow reshaping in deterministic networks with aggregate scheduling. With this regulator, packets of multiple flows are processed in one FIFO queue; the packet at the head of the queue is examined against the regulation constraints of its flow; it is released at the earliest time at which this is possible without violating the constraints. Packets that are not at the head of the queue are not examined until they reach the head of the queue. This regulator thus possibly delays the packet at the head of the queue but also all following packets, which typically belong to other flows. However, we show that, when it is placed after an arbitrary FIFO system, the worst case delay of the combination is not increased. This shaping-for-free property is well-known with per-flow shapers; surprisingly, it continues to hold here. To derive this property, we introduce a new definition of traffic regulator, the minimal Pi-regulator, which extends both the greedy shaper of network calculus and Chang's max-plus regulator and also includes new types of regulators such as packet rate limiters. Incidentally, we provide a new insight on the equivalence between min-plus and max-plus formulations of regulators and shapers.

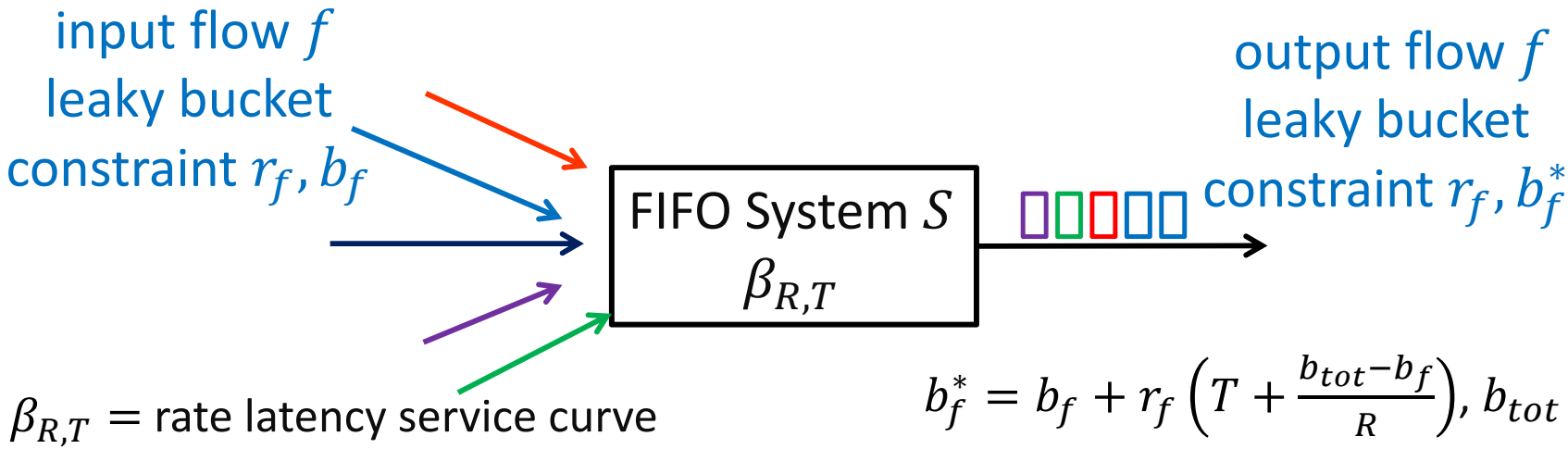
[Le Boudec 2018] Le Boudec, Jean-Yves, “A Theory of Traffic Regulators for Deterministic Networks with Application to Interleaved Regulators”, *arXiv preprint arXiv:1801.08477*.

1. FIFO Per-Class Networks

FIFO per class are commonly used in Time Sensitive Networking (IEEE 802.1 TSN, IETF Detnet).

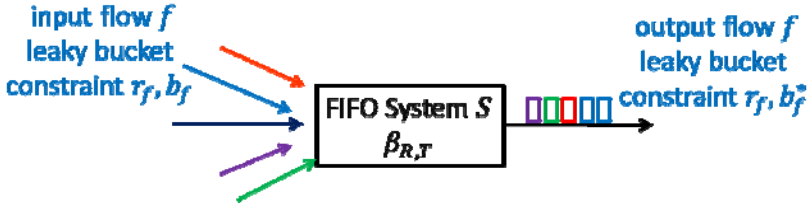
Computing backlog and delay bounds is hard [Boyer et al 2012] [Bouillard-Stea 2015][Bondorf et al 2017].

Example: [Le Boudec-Thiran 2001, Section 6.4]



Burstiness Cascade

Burstiness of every flow increases at every hop as a function of other flows' burstiness:



$$b_f^* = b_f + r_f\left(T + \frac{b_{tot} - b_f}{R}\right), \quad b_{tot} = \sum_i b_i$$

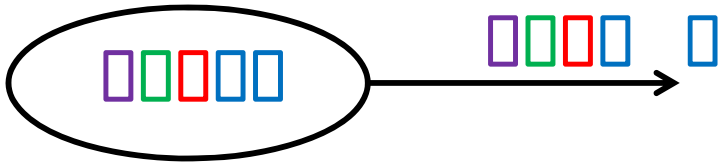
Increased burstiness causes increased burstiness (cascade).

Good delay bounds depend on the topology and on the number of hops. In non-feedforward nets, delay bounds are generally bad except at low utilizations and small numbers of hop [Bennett et al 2002].

Avoiding Burstiness Cascade

Solution 1: re-shape every flow at every hop (per-flow shaping)
Solves the problem but defeats the purpose of per-class network.

Solution 2: Interleaved Regulator



- FIFO queue of all packets of all flows in class
- packet at head of queue is examined versus traffic regulation of its flow; this packet is delayed if it came too early
- packets not at head of queue wait for their turn to come

[Specht-Samii 2016] “Urgency Based Scheduler”, now called “Asynchronous Traffic Shaping” at IEEE TSN

[Specht and Samii 2016] compute delay bounds for FIFO networks with interleaved regulators, using trajectory analysis.

Question 1: what can we say of worst-case delay due to Interleaved Regulator ?

[Specht-Samii 2016] considers two types of traffic rules

1. Leaky Bucket rule : Arrival curve $\sigma(t) = rt + b$ (min-plus calculus)
2. LRQ-rule: $A_n \geq A_{n-1} + \frac{L_{n-1}}{r}$
   (A_n: arrival time of packet n, L_n: length of packet n)
   LRQ-rule is a g-regulator as defined by C-S Chang (max-plus calculus) [Chang-Lin 1998]

LRQ is not an arrival curve; arrival curve is not a g-regulator.

Question 2: can we make a theory of interleaved shaper that applies both to arrival curve and g-regulator ?

2. Pi-Regulation

A single packet flow (A, L)

$A = (A_1, A_2, \dots)$ packet arrival times, $A \in \mathcal{F}_{inc}$

$L = (L_1, L_2, \dots)$ packet lengths

Π a mapping $(A, L) \to \Pi(A, L) = (E_1, E_2, \dots) \in \mathcal{F}$ (eligibility times)

This flow is Π-regular $\Leftrightarrow A \geq \Pi(A, L)$ i.e. $A_n \geq E_n$

We require that Π is causal (E_n depends only on $A_1, \dots, A_{n-1}$ and $L_1, \dots, L_n$), homogeneous (invariant by change of time origin) and isotone (if $A \geq A'$ then $\Pi(A, L) \geq \Pi(A', L)$).

Chang's g-regularity

Flow (A, L) is g-regular $\Leftrightarrow A_n - A_m \geq g(L_m + \cdots + L_{n-1})$
[Chang-Lin 1998] [Chang 2002]

This is Π-regulation with

$$\Pi(A, L)_n = \max_{1 \leq m \leq n-1} \{A_m + g(L_m + \cdots + L_{n-1})\}$$

LRQ-rule is a special case:

$$\Pi^{LRQ(r)}(A, L)_n = A_{n-1} + \frac{L_{n-1}}{r}$$
$$\Pi^{LRQ(r)}(A, L)_1 = -\infty$$

Max-Plus and Arrival Curve Constraints

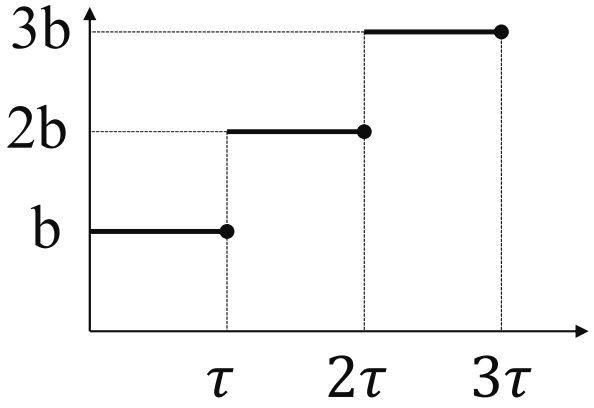
We need a max-plus formulation of arrival curve constraints.

Min-plus / max-plus duality is solved by Liebeherr [Liebeherr 2017] who shows the following equivalence:

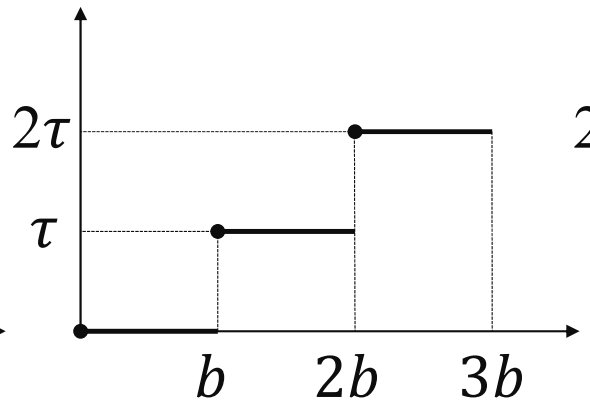
Min-plus	Max-plus
Cumulative arrival function $R(t) = \sum_n A_n 1_{A_n<t}$	Arrival time function $T(x) = \inf_n \left(A_n 1_{L_1+..+L_n>x}\right)$
Arrival curve $\sigma(t)$ $R(t) - R(s) \leq \sigma(t)$	Max-plus traffic enveloppe $\lambda(x)$ $T(y) - T(x) \geq \lambda(y-x)$
$T = R^{\uparrow}, \lambda = \sigma^{\uparrow}$	

Upper and Lower Pseudo-Inverses

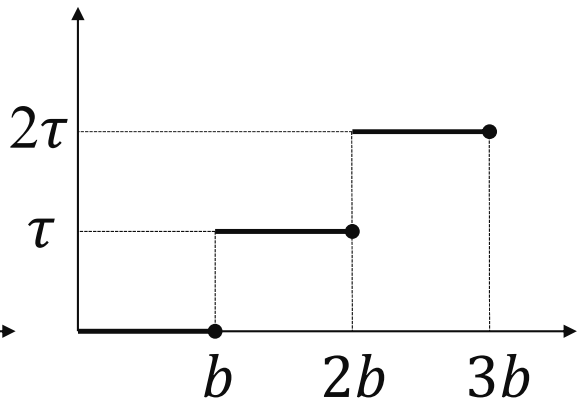
$$f^{\uparrow}(x) = \sup\{t, f(t) \leq x\} \qquad f^{\downarrow}(x) = \inf\{t, f(t) \geq x\}$$



$$\sigma(t) = b\left\lceil \frac{t}{\tau} \right\rceil$$



$$\sigma^{\uparrow}(x) = \tau\left\lfloor \frac{x}{b} \right\rfloor$$



$$\sigma^{\downarrow}(x) = \tau\left\lceil \frac{x}{b} - 1 \right\rceil$$

for $x > 0$

Recap

arrival curve can be expressed with max-plus traffic envelope

g-regulation (e.g. LRQ) uses max-plus but cannot be expressed as arrival curve

the problem is not min-plus versus max-plus, but viewpoint: observe flow at an arbitrary point in time (or bit) versus observe at packet arrival time

Viewpoint Equivalence Theorem max-plus formulation

Theorem: For a flow (A, L) the three conditions are equivalent

1. Flow has arrival curve constraint σ
2. $L_m + \cdots + L_n \leq \sigma^+(A_n - A_m)$
3. $A_n - A_m \geq \sigma^\downarrow(L_m + \cdots + L_n)$

$\sigma^+(t) = \lim_{s \to t, s > t} \sigma(s)$ (right-limit)

Viewpoint Equivalence Theorem max-plus formulation

For a flow (A, L) the three conditions are equivalent

1. Flow has max-plus traffic envelope λ
2. $L_m + \cdots + L_n \leq \lambda^{\uparrow}(A_n - A_m)$
3. $A_n - A_m \geq \lambda^{-}(L_m + \cdots + L_n)$

$\lambda^{-}(x) = \lim_{y \to x, y < x} \lambda(y)$ (left-limit)

Recall that $\lambda = \sigma^{\uparrow}$. Furthermore $\lambda^{\uparrow} = \sigma^{+}, \lambda^{-} = \sigma^{\downarrow}$

Arrival Curve as Pi-regulation

Arrival curve constraint σ is equivalent to Π-regularity with

$$\Pi(A, L) = \max_{1 \le m \le n-1} \{A_m + \sigma^{\downarrow}(L_m + \cdots + L_n)\}$$

e.g. Leaky bucket constraint

$$\Pi^{LB(r,b)}(A, L) = \max_{1 \le m \le n-1} \left\{A_m + \frac{L_m + \cdots + L_n - b}{r}\right\}$$

e.g. Staircase arrival curve

$$\Pi^{SC(\tau,b)}(A, L) = \max_{1 \le m \le n-1} \left\{A_m + \tau \left\lceil \frac{L_m + \cdots + L_n - b}{b} \right\rceil\right\}$$

IEEE TSN Traffic Regulation Constraint

At most K packets in an interval of τ seconds.

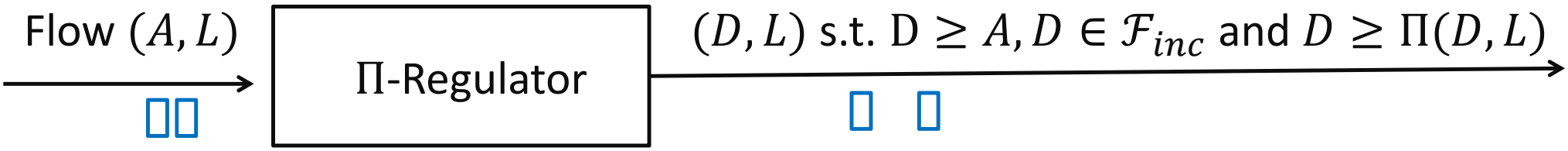
This is Π-regularity with

$$\Pi^{TSN(\tau,K)}(A,L) = \max_{1\leq m\leq n-1}\left\{A_m + \tau\left\lceil\frac{n-m+1-K}{K}\right\rceil\right\}$$

This is neither an arrival curve constraint nor g-regulation.

Other packet rate limits can be expressed as Pi-regulation (e.g. min spacing between packets, e.g. affine constraints)

Per-flow Minimal Pi-Regulator



Π-Regulator is FIFO and transforms a flow into a Π-regular flow.

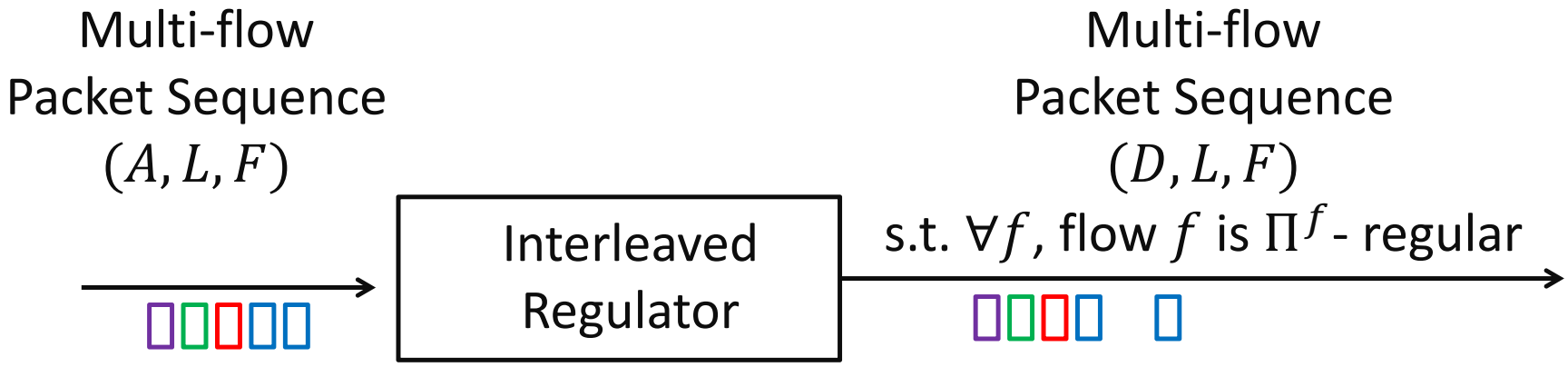
There is one Minimal Π-Regulator; it is defined by $D_1 = A_1$ and

$$D_n = \max\{A_n, D_{n-1}, \Pi(D)_n\}$$

If regulation is "arrival curve constraint" the minimal Π-regulator is the packetized greedy shaper.

If regulation is "g-regulation" it is the minimal g-regulator.

3. Interleaved Regulator



A_n: arrival time of packet n; L_n: length; F_n: flow id of packet n

An Interleaved regulator is a FIFO system such that every output flow f is Π^f - regular

$$D^f \geq \Pi^f\left(D^f, L^f\right)$$

where D^f is the subsequence of D obtained by keeping only dates that correspond to packets of flow f

Minimal Interleaved Regulator

Theorem: There is one minimal interleaved regulator (i.e. such that $D_n \leq D'_n$ for any other interleaved regulator).

It is given by $D_1 = A_1$ and

$$D_n = \max\left\{A_n, D_{n-1}, \Pi^{F_n}\left(D^{F_n}, L^{F_n}\right)_{I(n)}\right\}$$

where $I(n)$ is the index of packet n in its flow.

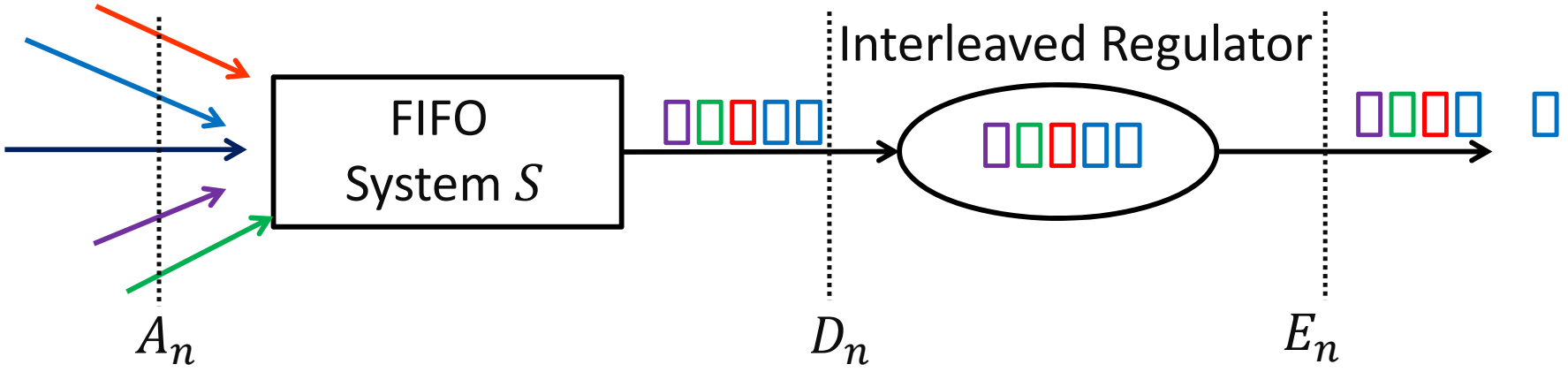
Implementation of Minimal Interleaved Regulator

$$D_n = \max\left\{A_n, D_{n-1}, \Pi^{F_n}\left(D^{F_n}, L^{F_n}\right)_{I(n)}\right\}$$

Eligibility Time of packet at head of queue

- One FIFO queue for all packets of all flows.
- Packet at head of queue is examined and delayed until it can be released while satisfying the regulation of its flow.
- Other packets wait until their turn comes.

Interleaved Regulator Does Not Increase Worst Case Delay



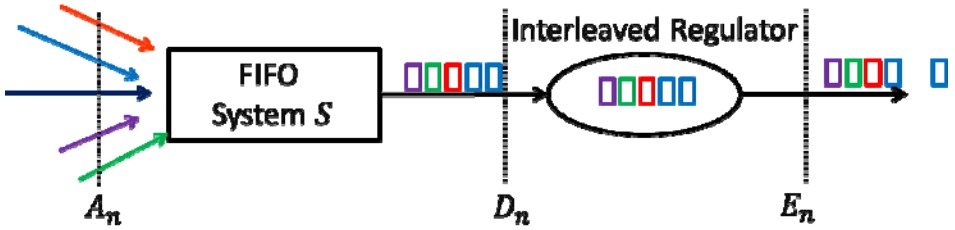
Every flow f is Π^f regular before input to S

Output of S is fed to interleaved regulator with regulator Π^f for flow f

Theorem: $\sup_n(D_n - A_n) = \sup_n(E_n - A_n)$

Interleaved Regulator is for free !

Proof Outline

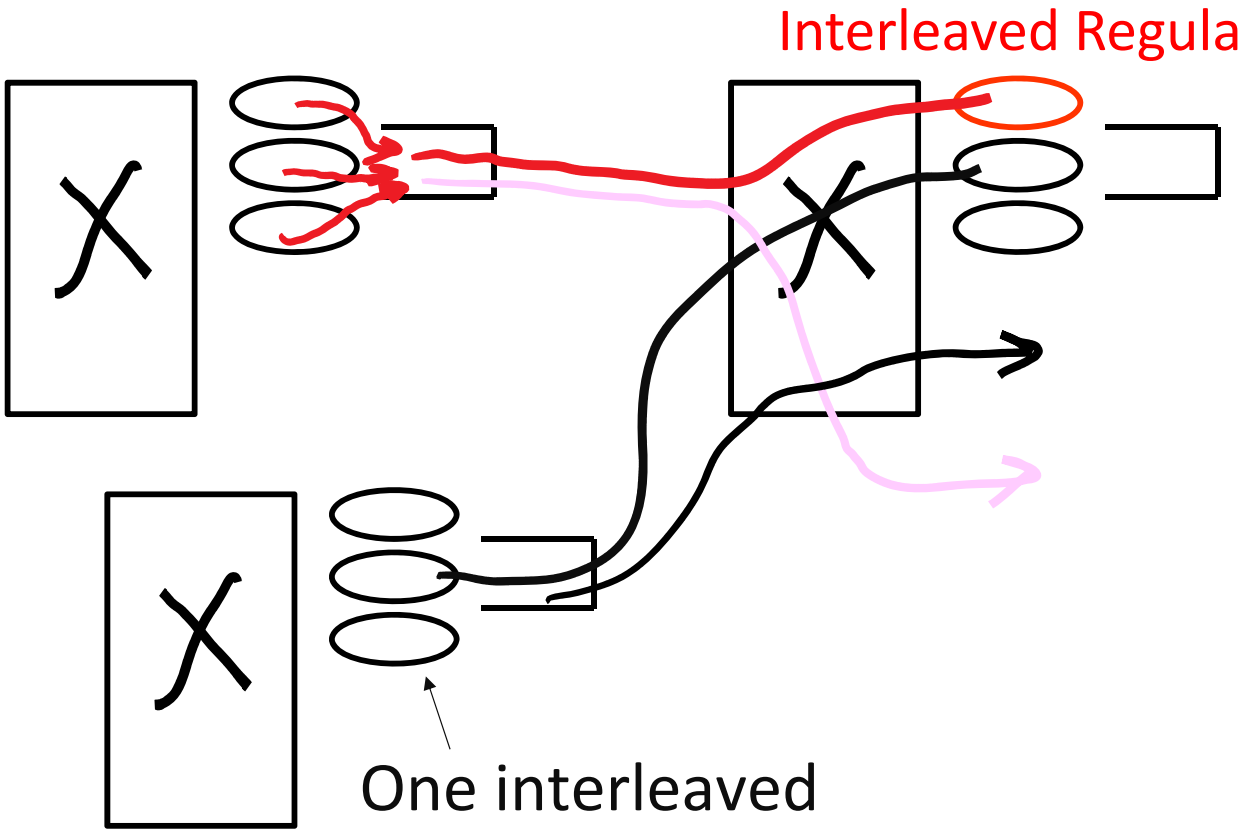


Show by induction that $E_n \leq A_n + d$ for any delay bound d on S. Fix n and let $f = F_n, i = I(n)$ so that $A_n = A_i^f$ and $E_n = \max\left\{A_n, E_{n-1}, \Pi^f\left(E^f, L^f\right)_i\right\}$. Show each term is $\leq A_n + d$

1. $A_n \leq A_n + d$ because $d \geq 0$
2. $E_{n-1} \leq A_{n-1} + d$ (induction) $\leq A_n + d$
3. $E_j^f \leq A_j^f + d$ for $j < i$ (induction) thus (Π^f is causal, isotone, homog.) $\Pi^f\left(E^f\right)_i \leq \Pi^f\left(A^f + d\right)_i = \Pi^f\left(A^f\right)_i + d$

   (A, L) is Π^f-regular $\Rightarrow \Pi^f\left(A^f\right)_i + d \leq A_i^f + d = A_n + d$

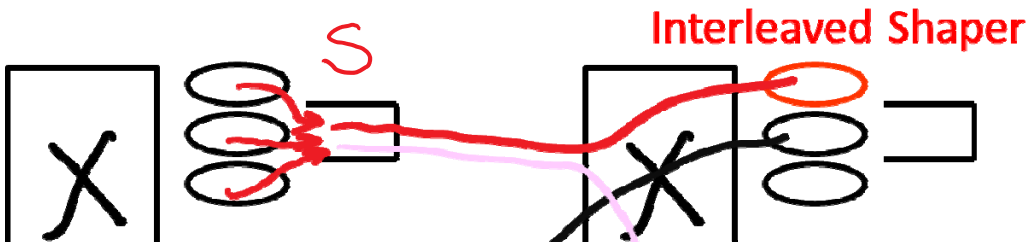
FIFO Network With Interleaved Regulators



[Specht-Samii 2016] places one interleaved regulator per input port before output queue.

Output of interleaved regulator has known burstiness
⇒ no burstiness cascade.

Delay Computations in IEEE TSN



- Apply theorem where S = output scheduler at previous hop
- Worst case end-to-end queuing delay can ignore interleaved regulators. Delay bound at one interleaved regulator is absorbed by delay at previous hop.
- Queuing delay at every scheduler S (without shaper) can be computed easily since traffic is regular.
- Worst case delay at one node cannot ignore interleaved shaper.
  ⇒ Worst case end-to-end delay is generally less than sum of per-hop delays.

Conclusions

Interleaved Regulators can be used to simplify and control FIFO networks.

Shaping-for-free is known for per-flow networks. Also holds for FIFO networks with interleaved regulators.

Pi-regulation generalizes arrival curves, g-regulation, packet rate limitations.

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